PCN
Product/Process Change Notification

Industrial grade qualification of 600W TVS in SMA package at additional Assembly/Test line at subcontractor in China

Notification number:	ADG-DIS/20/12216	**Issue Date**	22/06/2020
Issued by	Aline AUGIS		
Product series affected by the change		SMA 600W TVS unidirectional products • 12V <= VRM <= 33V, • SMA6J12A-TR to SMA6J33A-TR	
Type of change		Additional assembly line on existing qualified Back end, for increased production capacity	

Description of the change

STMicroelectronics is qualifying an additional assembly line of its 600W TVS products in **SMA** package at existing subcontractor in **China**.

Reason for change

STMicroelectronics has decided to expand the manufacturing capacity of TVS protection devices housed in SMA package. This additional assembly line is located in China in a subcontractor already qualified and delivering in high volume for ST.

Former versus changed product:	The changed products will remain fully compliant with product datasheet in term of electrical, dimensional or thermal parameters. The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged. The footprint recommended by ST remains the same. There is no change in packing modes and standard delivery quantities either. The products remain in full compliance with the ST ECOPACK®2 grade (“halogen-free”).

Disposition of former products

Purpose is to implement additional production capacity; shipments will be done from all qualified assembly lines.

Marking and traceability

Marking is

Assembly location	Plant and date code		
	Assy plant code	Assy year	Assy week
China (subco current line)	GP	**Y** (1 digit indicating the year)	**WW** (2 digits indicating the week number)
China (subco new line)	**GP**		

Traceability for the implemented change will be ensured by an **internal codification** and by the **Q.A. number**.

Qualification complete date	2020 week 23

Forecasted sample availability

Product family	Sub-family	Commercial part Number	Availability date
Protection device	TVS	SMA6J12A-TR	W28-2020
		SMA6J13A-TR	W28-2020
		SMA6J15A-TR	W28-2020
		SMA6J18A-TR	W28-2020
		SMA6J20A-TR	W28-2020
		SMA6J24A-TR	W28-2020
		SMA6J26A-TR	W28-2020
		SMA6J28A-TR	W28-2020
		SMA6J33A-TR	Immediate

Change implementation schedule

Sales types	Estimated production start	Estimated first shipments
All	W37-2020	W39-2019

Comments:	With early PCN acceptance, possible shipment starting week 27 on selected part numbers.

Customer's feedback

Please contact your local ST sales representative or quality contact for requests concerning this change notification.
Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change
Absence of additional response within 90 days of receipt of this PCN will constitute acceptance of the change

Qualification program and results	20029QRP Attached

Reliability Evaluation Report

SMA6Jxx (VRM from 5V to 33V) product qualification

General Information	
Product Description	*Protection*
Finish Good(s)	*SMA6J5.0A-TR / CA-TR* *SMA6J6.0A-TR / CA-TR* *SMA6J6.5A-TR / CA-TR* *SMA6J8.5A-TR / CA-TR* *SMA6J10A-TR / CA-TR* *SMA6J12A-TR / CA-TR* *SMA6J13A-TR / CA-TR* *SMA6J15A-TR / CA-TR* *SMA6J18A-TR / CA-TR* *SMA6J20A-TR / CA-TR* *SMA6J24A-TR / CA-TR* *SMA6J26A-TR / CA-TR* *SMA6J28A-TR / CA-TR* *SMA6J33A-TR / CA-TR*
Product Group	*ADG*
Product division	*DFD*
Package	*SMA*
Maturity level step	*QUALIFIED*

Locations	
Wafer fab	*ST TOURS FRANCE*
Assembly plant	*SUBCONTRACTOR IN CHINA 9941*
Reliability Lab	*ST TOURS FRANCE*

Reliability Assessment
PASS

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1	28/05/2020	8	Aude DROMEL	Julien MICHELON	Initial release

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

ST Restricted

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS 3
2 GLOSSARY 3
3 RELIABILITY EVALUATION OVERVIEW 3
3.1 OBJECTIVES 3
3.2 CONCLUSION 3
4 DEVICE CHARACTERISTICS 4
4.1 DEVICE DESCRIPTION 4
4.2 CONSTRUCTION NOTE 5
5 TESTS RESULTS SUMMARY 5
5.1 TEST VEHICLES 5
5.2 TEST PLAN AND RESULTS SUMMARY 6
6 ANNEXES 7
6.1 TESTS DESCRIPTION 7

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices

2 GLOSSARY

SS	Sample Size
PC	Pre-conditioning
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
THB / H3TRB	Thermal Humidity Bias
UHAST	Unbiased Highly Accelerated Stress Test
DBT	Dead Bug Test

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

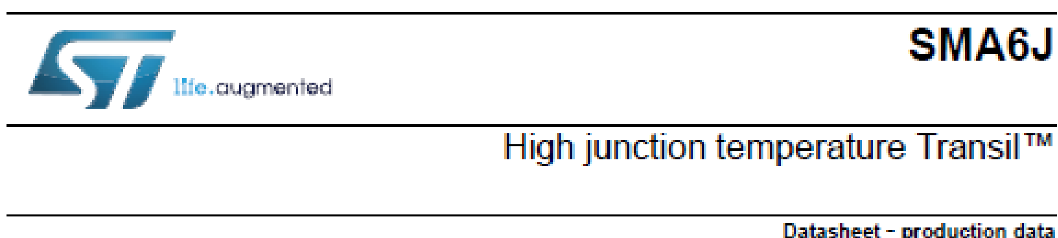
The objective is to qualify SMA package at our subcontractor in China for 600W protection devices from 5V to 33V (VRM).

3.2 Conclusion

Qualification plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

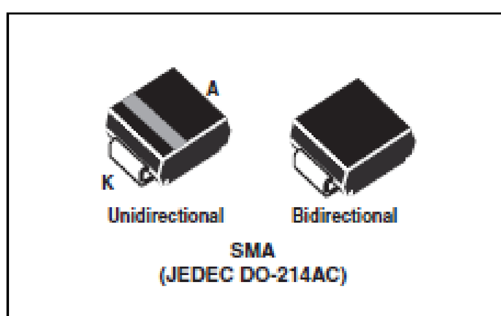
4.1 Device description



SMA6J

High junction temperature Transil™

Datasheet - production data



Features

- Peak pulse power:
  - 600 W (10/1000 µs)
  - 4 kW (8/20 µs)
- Stand off voltage range: from 5 V to 188 V
- Unidirectional and bidirectional types
- Low clamping voltage versus standard series
- Low leakage current:
  - 0.2 µA at 25 °C
  - 1 µA at 85 °C
- Operating T_j max: 175 °C
- JEDEC registered package outline

Complies with the following standards

- IEC 61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883G-Method 3015-7: class3B
  - 25 kV (human body model)

Description

The SMA6J Transil series has been designed to protect sensitive equipment against electro-static discharges according to IEC 61000-4-2, MIL STD 883 Method 3015, and electrical over stress such as IEC 61000-4-4 and 5. They are generally for surges below 600 W 10/1000 µs.

This planar technology makes it compatible with high-end equipment and SMPS where low leakage current and high junction temperature are required to provide reliability and stability over time. Their low clamping voltages provides a better safety margin to protect sensitive circuits with extended life time expectancy.

Packaged in SMA, this minimizes PCB space consumption (SMA footprint in accordance with IPC 7531 standard).

4.2 Construction note

	SMA6JxxA-TR / CA-TR (xx VRM from 5V to 33V)
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS GLOBAL 6"
Technology / Process family	DISCRETE-TRANSIL / TAN
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST TOURS FRANCE
Assembly information	
Assembly site	SUBCONTRACTOR IN CHINA
Package description	SMA
Final testing information	
Testing location	SUBCONTRACTOR IN CHINA

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

<table>
<tr><th>Lot #</th><th>Part Number</th><th>Die manufacturing plant</th><th>Assembly plant</th><th>Package</th><th>Comments</th></tr>
<tr><td>Lot 1</td><td>SMA6J5.0A-TR</td><td rowspan="4">ST TOURS</td><td rowspan="4">SUBCONTRACTOR CHINA</td><td rowspan="4">SMA</td><td rowspan="3">Qualification lots</td></tr>
<tr><td>Lot 2</td><td>SMA6J33A-TR</td></tr>
<tr><td>Lot 3</td><td>SMA6J33CA-TR</td></tr>
<tr><td>Lot 4</td><td>SMA6T39CAY</td><td>Similar package for solderability trials</td></tr>
</table>

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	Total	Steps	Results/Lot Fail/S.S.		
						Lot 1	Lot 2	Lot 3
Die Oriented Tests								
Repetitive Surge	Y	ADCS0060282	IPP=Ref DS Pulse delay=0.01ms	60	measure at 50s	0/20	0/20	0/20
					measure at 1000s	0/20	0/20	0/20
HTRB	N	JESD22-A108/MIL-STD-750-1 M1038 Method A	Junction Temperature=175°C Tension=VRM	231	504h	0/77	0/77	0/77
					1000h	0/77	0/77	0/77
Package Oriented Tests								
TC	Y	JESD22-A104	Frequency (cy/h)=2cy/h Temperature (high)=150°C Temperature (low)=-55°C	77	500cy	-	0/77	-
					1000cy	-	0/77	-
THB/H3TRB	Y	JESD22-A101	Humidity (HR)=85% Temperature=85°C Tension=33V	77	168h	-	0/77	-
					504h	-	0/77	-
					1000h	-	0/77	-
UHAST	Y	JESD22 A-118	Humidity (HR)=85% Pressure=2.3bar Temperature=130°C	77	96h	-	-	0/77

For solderability oriented trials similarities are done with the ASMA6T39CAYH/NS (same package) :

Test	PC	Std ref.	Conditions	SS	Steps	Failure /SS
						Lot 4
Solderability	N	J-STD-002	Steam Ageing SnAgCu bath 245°C	60	Visual inspection	0/15
			Steam Ageing SnPb 220°C			0/15
			Dry Ageing SnAgCu 245°C			0/15
			Dry Ageing SnPb 220°C			0/15
DBT	N	DM 00112629	Fluxing followed by IR reflow.	30	Visual inspection	0/30

6 ANNEXES

6.1 Tests Description

Test name	Standard Reference	Description	Purpose
Die Oriented			
HTRB High Temperature Reverse Bias	JESD22 A-108	HTRB : High Temperature Reverse Bias HTFB / HTGB : High Temperature Forward (Gate) Bias The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - low power dissipation; - max. supply voltage compatible with diffusion process and internal circuitry limitations.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Repetitive surges	ADCS0060282	Devices are submitted to rated Ipp for 1000 surges.	Purpose: This test is intended to verify robustness of device submitted to rated Ipp (as per data sheet) = exploration of reverse characteristic at a calibrated current value followed by the measure of voltage clamping value. Failure mode expected is short circuit of the device due to hot spot creation into silicon bulk at device periphery where the electrical field gradient is the most important. Physical analysis must be done to verify consistency of the failure mode and discriminate from extrinsic causes related to process escapes.
Package Oriented			
TC Temperature Cycling	JESD22 A-104	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
PC Preconditioning	JESD22 A-113	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

Test name	Standard Reference	Description	Purpose
THB/H3TRB Temperature Humidity Bias	JESD22 A-101	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
uHAST	JESD22 A-118	The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solidstate devices in humid environments .	Purpose: to investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. To point out critical water entry paths with consequent electrochemical and galvanic corrosion.
Solderability	J-STD-002	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.
DBT	DM00112629	To evaluate the wettability of the SMD. Good indicator to determine the bad solderability behavior	Components are glued up-side down on a substrate. Pins are wetted with a moderately activated flux. Then run once through the reflow oven with leadfree temperature profile. Visual inspection is performed with suitable tool.